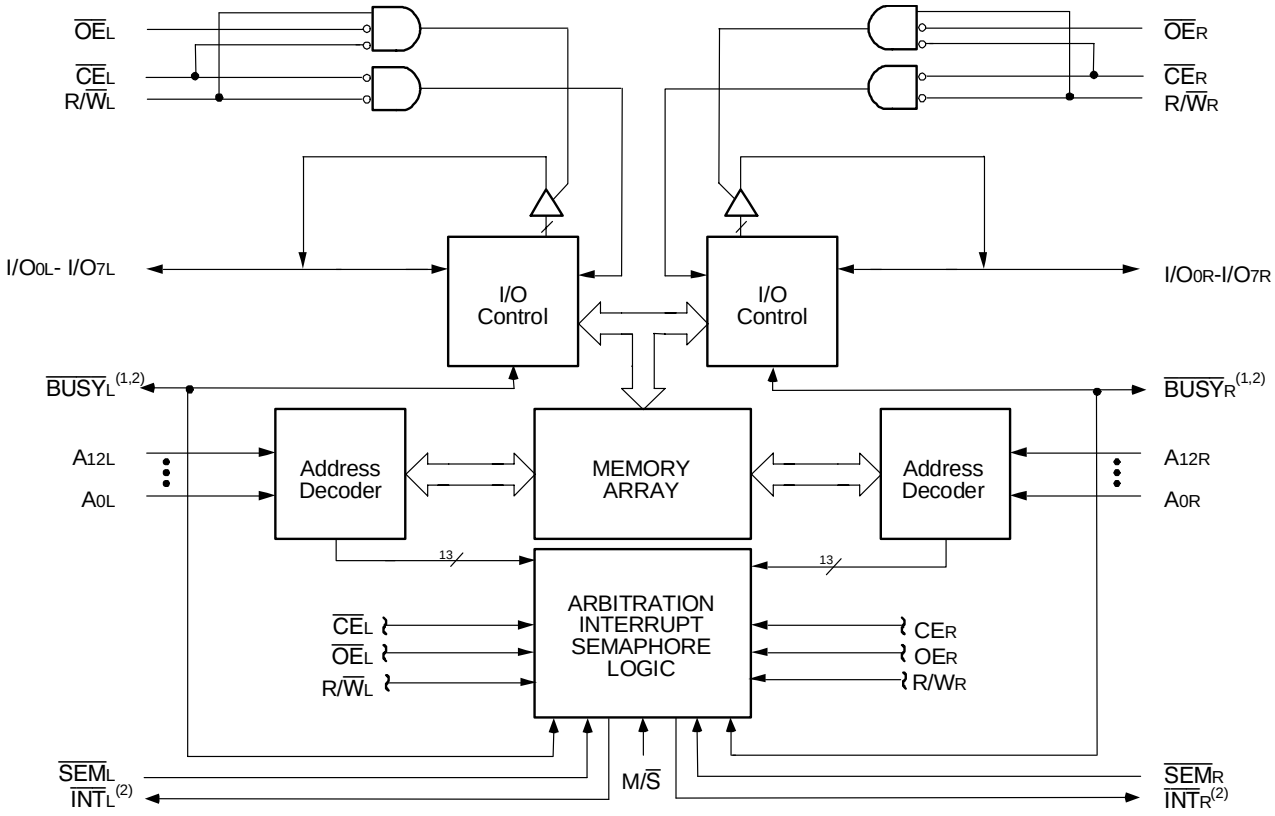
HIGH-SPEED 3.3V 8K x 8 DUAL-PORT STATIC RAM

IDT70V05S/L

Features

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **High-speed access**
  - *Commercial: 15/20/25/35/55ns (max.)*
  - *Industrial: 20ns (max.)*
- **Low-power operation**
  - *IDT70V05S*
    Active: 400mW (typ.)
    Standby: 3.3mW (typ.)
  - *IDT70V05L*
    Active: 380mW (typ.)
    Standby: 660µW (typ.)
- **IDT70V05 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device**
- **M/$\overline{S}$ = VIH for $\overline{BUSY}$ output flag on Master**
  M/$\overline{S}$ = VIL for $\overline{BUSY}$ input on Slave
- **Interrupt Flag**
- **On-chip port arbitration logic**
- **Full on-chip hardware support of semaphore signaling between ports**
- **Fully asynchronous operation from either port**
- **TTL-compatible, single 3.3V (±0.3V) power supply**
- **Available in 68-pin PGA and PLCC, and a 64-pin TQFP**
- **Industrial temperature range (-40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram



2942 drw 01

NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

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Description

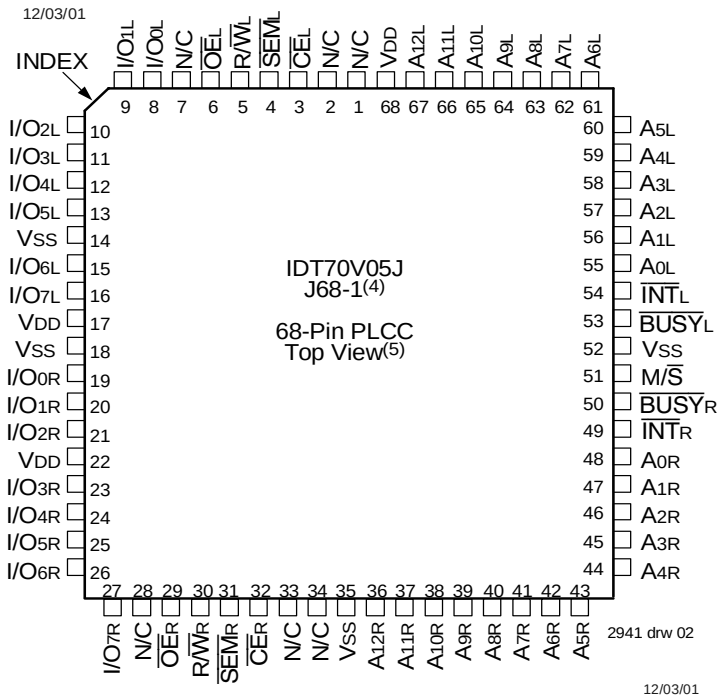
The IDT70V05 is a high-speed 8K x 8 Dual-Port Static RAM. The IDT70V05 is designed to be used as a stand-alone 64K-bit Dual-Port SRAM or as a combination MASTER/SLAVE Dual-Port SRAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port SRAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

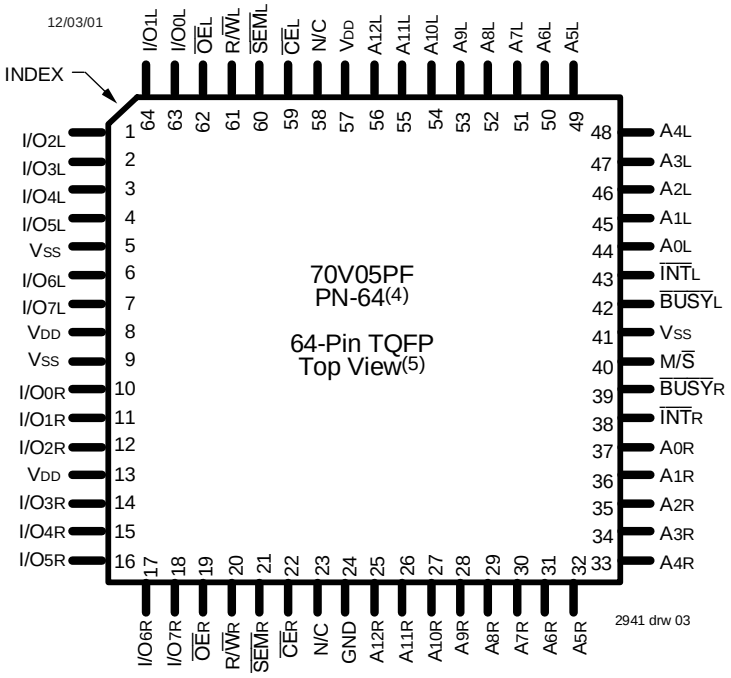
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 400mW of power.

The IDT70V05 is packaged in a ceramic 68-pin PGA and PLCC and a 64-pin thin quad flatpack (TQFP).

Pin Configurations[1,2,3]





NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. J68-1 package body is approximately .95 in x .95 in x .17 in.
   PN64 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

2941 tbl 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 0.3V.

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2941 tbl 07

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitznce when the input and output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

2941 tbl 05

NOTE:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2941 tbl 06

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{DD} +0.3V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V05S		70V05L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{DD} = 3.6V, V_{IN} = 0V to V_{DD}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{DD}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2941 tbl 08

NOTE:
1. At $V_{DD} \leq$ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1] (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V05X15 Com'l Only Typ.[2]	70V05X15 Com'l Only Max.	70V05X20 Com'l & Ind Typ.[2]	70V05X20 Com'l & Ind Max.	70V05X25 Com'l Only Typ.[2]	70V05X25 Com'l Only Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled SEM = V_{IH} f = f_{MAX}[3]	COM'L	S	150	215	140	200	130	190	mA
				L	140	185	130	175	125	165	
			IND	S	—	—	140	225	—	—	mA
				L	—	—	130	195	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L	S	25	35	20	30	16	30	mA
				L	20	30	15	25	13	25	
			IND	S	—	—	20	45	—	—	mA
				L	—	—	15	40	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ = V_{IH} Active Port Outputs Disabled, f=f_{MAX}[3]	COM'L	S	85	120	80	110	75	110	mA
				L	80	110	75	100	72	95	
			IND	S	—	—	80	130	—	—	mA
				L	—	—	75	115	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V	COM'L	S	1.0	5	1.0	5	1.0	5	mA
				L	0.2	2.5	0.2	2.5	0.2	2.5	
			IND	S	—	—	1.0	15	—	—	mA
				L	—	—	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{DD} - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled, f = f_{MAX}[3]	COM'L	S	85	125	80	115	75	105	mA
				L	80	105	75	100	70	90	
			IND	S	—	—	80	130	—	—	mA
				L	—	—	75	115	—	—	

2941 tbl 09a

Symbol	Parameter	Test Condition	Version		70V05X35 Com'l Only Typ.[2]	70V05X35 Com'l Only Max.	70V05X55 Com'l Only Typ.[2]	70V05X55 Com'l Only Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled SEM = V_{IH} f = f_{MAX}[3]	COM'L	S	120	180	120	180	mA
				L	115	155	115	155	
			IND	S	120	200	120	200	mA
				L	115	170	115	170	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L	S	13	25	13	25	mA
				L	11	20	11	20	
			IND	S	13	40	13	40	mA
				L	11	35	11	35	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ = V_{IH} Active Port Outputs Disabled, f=f_{MAX}[3]	COM'L	S	70	100	70	100	mA
				L	65	90	65	90	
			IND	S	70	120	70	120	mA
				L	65	105	65	105	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V	COM'L	S	1.0	5	1.0	5	mA
				L	0.2	2.5	0.2	2.5	
			IND	S	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{DD} - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled, f = f_{MAX}[3]	COM'L	S	65	100	65	100	mA
				L	60	85	60	85	
			IND	S	65	115	65	115	mA
				L	60	100	60	100	

2941 tbl 09b

NOTES:

1. "X" in part number indicates power rating (S or L)
2. V_{DD} = 3.3V, T_A = +25°C, and are not production tested. $I_{DD\,DC}$ = 115mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[4]

Symbol	Parameter	70V05X15 Com'l Only		70V05X20 Com'l & Ind		70V05X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACE}	Chip Enable Access Time[3]	—	15	—	20	—	25	ns
t_{AOE}	Output Enable Access Time[3]	—	10	—	12	—	13	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	10	—	12	—	15	ns
t_{PU}	Chip Enable to Power Up Time[1,2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[1,2]	—	15	—	20	—	25	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—	ns
t_{SAA}	Semaphore Address Access[3]	—	15	—	20	—	25	ns

2941 tbl 11a

Symbol	Parameter	70V05X35 Com'l Only		70V05X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	35	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time[3]	—	35	—	55	ns
t_{AOE}	Output Enable Access Time[3]	—	20	—	30	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	25	ns
t_{PU}	Chip Enable to Power Up Time[1,2]	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[1,2]	—	35	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
t_{SAA}	Semaphore Address Access[3]	—	35	—	55	ns

2941 tbl 11b

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is determined by device characterization but is not production tested.
3. To access SRAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
4. 'X' in part number indicates power rating (S or L).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(5)

Symbol	Parameter	70V05X15 Com'l Only		70V05X20 Com'l & Ind		70V05X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	15	—	15	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	12	—	15	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	10	—	12	—	15	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

2941 tbl 12a

Symbol	Parameter	70V05X35 Com'l Only		70V05X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	30	—	45	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	45	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	30	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	15	—	25	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	15	—	25	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

2941 tbl 12b

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is determined by device characterization but is not production tested.
3. To access SRAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. "X" in part number indicates power rating (S or L).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(6)

Symbol	Parameter	70V05X15 Com'l Ony		70V05X20 Com'l & Ind		70V05X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/S = VIH)								
tBAA	BUSY Access Time from Address Match	—	15	—	20	—	20	ns
tBDA	BUSY Disable Time from Address Not Matched	—	15	—	20	—	20	ns
tBAC	BUSY Access Time from Chip Enable LOW	—	15	—	20	—	20	ns
tBDC	BUSY Disable Time from Chip Enable HIGH	—	15	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data(3)	—	18	—	30	—	30	ns
tWH	Write Hold After BUSY(5)	12	—	15	—	17	—	ns
BUSY TIMING (M/S = VIL)								
tWB	BUSY Input to Write(4)	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY(5)	12	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay(1)	—	30	—	45	—	50	ns
tDDD	Write Data Valid to Read Data Delay(1)	—	25	—	35	—	35	ns

2941 tbl 13a

Symbol	Parameter	70V05X35 Com'l Only		70V05X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (M/S = VIH)						
tBAA	BUSY Access Time from Address Match	—	20	—	45	ns
tBDA	BUSY Disable Time from Address Not Matched	—	20	—	40	ns
tBAC	BUSY Access Time from Chip Enable LOW	—	20	—	40	ns
tBDC	BUSY Disable Time from Chip Enable HIGH	—	20	—	35	ns
tAPS	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data(3)	—	35	—	40	ns
tWH	Write Hold After BUSY(5)	25	—	25	—	ns
BUSY TIMING (M/S = VIL)						
tWB	BUSY Input to Write(4)	0	—	0	—	ns
tWH	Write Hold After BUSY(5)	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay(1)	—	60	—	80	ns
tDDD	Write Data Valid to Read Data Delay(1)	—	45	—	65	ns

2941 tbl 13b

NOTES:
1. Port-to-port delay through SRAM cells from writing port to reading port, refer to "Timing Waveform of Read With BUSY (M/S = VIH)" or "Timing Waveform of Write With Port-To-Port Delay (M/S = VIL)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. 'X' is part number indicates power rating (S or L).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

		70V05X15 Com'l Only		70V05X20 Com'l & Ind		70V05X25 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	15	—	20	—	20	ns
t_{INR}	Interrupt Reset Time	—	15	—	20	—	20	ns

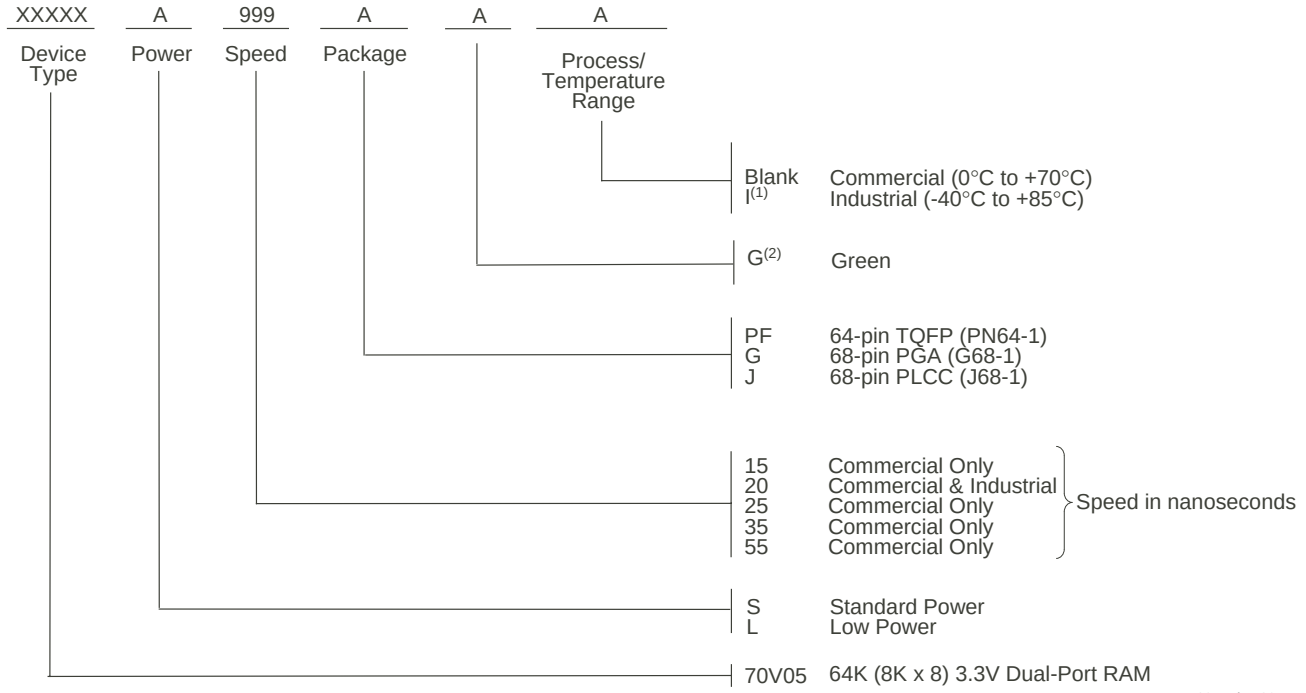
2941 tbl 14a

		70V05X35 Com'l Only		70V05X55 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING						
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	40	ns
t_{INR}	Interrupt Reset Time	—	25	—	40	ns

2941 tbl 14b

NOTES:
1. 'X' in part number indicates power rating (S or L).

Ordering Information



2941 drw 20

NOTE:

1. Contact your local sales office for Industrial temp range in other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.